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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,533	03/26/2004	Wan-Cheng Yang	N1085-00261	8951
54657	7590	11/16/2005	[TSMC2003-111]	
DUANE MORRIS LLP IP DEPARTMENT (TSMC) 30 SOUTH 17TH STREET PHILADELPHIA, PA 19103-4196			EXAMINER PERT, EVAN T	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/810,533

Applicant(s)

YANG, WAN-CHENG

Examiner

Evan Pert

Art Unit

2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 August 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The informal drawings are acceptable for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5-16 and 19-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Battal et al. (US 2005/0026542 A1).

Regarding claim 1, the Battal et al. reference discloses a method for mapping surface topography (e.g. a Ta barrier being polished away from surfaces of an ILD with vias) of a substrate (e.g. a semiconductor wafer) comprising: forming a non-metallic film (e.g. ILD 104) over a substrate; forming a metal film (e.g. Ta barrier over ILD 104 and in via openings before CMP of Ta barrier per [0053]) over said non-metallic film (i.e. Ta barrier is formed over ILD 108); polishing to remove at least a portion of said metal film (i.e. the Ta barrier is polished until removed from upper planar surfaces of ILD 104, yet left to remain as a lining of the via openings); and distinguishing first regions in which said metal film remains, from second regions in which said metal film has been removed and said non-metallic film is exposed (i.e. distinguishing per [0053]).

Regarding claim 2, the film 104 is ILD, which is "dielectric."

Regarding claim 3, Fig. 1 shows "further films" as claimed and as is well known in the art of semiconductor device manufacture.

Regarding claim 5, the polishing and distinguishing take place during in-line processing with probes that generate topographical data based on spectral signals from areas of the wafer where Ta barrier is not polished away [0028]-[0029]

Regarding claim 6, "copper" is "increasing in popularity" per [0003].

Regarding claim 7, CMP is the process of polishing [0005]

Regarding claims 8, 12 and 13, the top surface is monitored by an interferometer (i.e. a spectrometer) when the top surface is pressed against the polishing pad having probes facing the top wafer surface during CMP [see cover figure].

Regarding claims 9 and 10, the distinguishing is repeated by flashing a lamp during the process, which happens "periodically" yet as a pulse train of flashes, distinguishing can be said to be happening "continuously."

Regarding claim 11, regions are radially distinguished (as "bands") and a 3-D topographical map is generated by assumption that there is radial symmetry [0048].

Regarding claim 14, a map is generated for the topography [0048].

Regarding claim 15, in-line process controls are instituted based on undesirables in the map [0051].

Regarding claim 16, with dishing occurring at the via opening regions, the portion where Ta barrier is not removed is relatively depressed which is distinguished from non-via areas which are more planar [0036].

Regarding claim 19, the Battal et al. reference discloses a method for mapping surface topography of a substrate [0036] comprising: forming a non-reflective film [e.g. ILD 104] over a substrate (102), forming a reflective film over said non-reflective film (e.g. Ta barrier per [0053]; polishing to remove at least a portion of said reflective film (e.g. polishing by CMP to remove Ta barrier on upper horizontal surfaces of silicon oxide 104 per [0053]); and distinguishing first regions in which said reflective film remains (i.e. lining the vias), from second regions in which said reflective film has been removed and said non-reflective film is exposed (i.e. upper surface of oxide 104 is exposed when Ta barrier is polished away per [0053]).

Regarding claim 20, the Battal et al. reference discloses an apparatus for in-line monitoring of surface topography (cover figure) of a substrate (100) comprising : a body for receiving a substrate thereon (i.e. the body where wafer 100 is received seen in the cover figure), polishing means for polishing a surface of said substrate (i.e. CMP polishing pad 309), and detecting means for detecting a presence or absence of a reflective film at a plurality of locations on said surface during said polishing operation (e.g. probes 306a, 306b and 306c that detect presence or absence of reflective Ta barrier film as it is polished away from upper horizontal surfaces of oxide ILD 104 per [0053]).

Regarding claim 21, the probes are part of an optical system [0045].

Regarding claim 22, the means is an interferometer (i.e. a spectrometer type of interferometer).

Regarding claim 23, the polishing is a "CMP" [0005].

Regarding claim 24, the detecting means detects during specific times (e.g. light flashes), at multiple locations (i.e. many probes, more data), and so the probes distinguish "several times" at least.

Regarding claim 25, the output is displayed as a graph of spectral data correlating with surface topography made of the surfaces being polished.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 4, 17-18 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Battal et al. as applied to claims 1, 3, and 25 above, and further in view of Official Notice.

Claim 4

Regarding claim 4, the Battal et al. reference is silent about interconnects 108 being "patterned polysilicon."

The examiner takes Official Notice that patterned polysilicon was well known, prior to the filing of the Battal et al. application, for making a wiring layer such as wiring 108 wherein polysilicon can be electrically conductive and process compatible.

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It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to adopt “patterned polysilicon” as a layer for wiring because patterned polysilicon can be used in practicing the Battal et al. method because the polysilicon can be optically distinguished from other materials common in making an integrated circuit [0003], such as the ILD deposited over wiring 108 [MPEP 2144].

Claims 17-18

Regarding claims 17-18, the Battal et al. reference is silent about the probes' claimed spacing (i.e. “10-20 mm”) and the diameter of the wafer 100 being “12 inches”, as well as monitoring optical signals “directed to a plurality of scribe lines”.

The examiner takes Official Notice that optical test grating and CMP structures placed in scribe lines were well known prior to filing of the Battal et al. reference, since the scribe lines are unused space and test structures not useful for sale can be placed in the scribe lines and with the test structures being more sensitive to the process being monitored.

The spacing of probes is disclosed in the Battal et al. reference as “as many as possible” for the “best data,” and the 12 inch wafer size is becoming a new standard as admitted by applicant as admitted prior art.

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to adopt a standard wafer size (i.e. 12 inches) motivated by availability and commercial desirability, using scribe lines for sensitive test structures as is known in the art, motivated to save space for saleable devices between scribe lines, and would be motivated to space as many probes as possible, in accordance with the teachings of the Battal et al. reference such, that "10-20mm" offers nothing unexpected over the teachings of the Battal et al. reference (e.g. 10 mm spacing gives more data than 20 mm spacing) [MPEP 2144].

Claim 26

Regarding claim 26, the Battal et al. reference is silent about "electronic circuitry" that "compares output to pass/fail criteria" since the output is spectral data that is "utilized" for process improvement and/or feedback control.

The examiner takes Official Notice that automatic "electronic circuitry" that compares output results of a process measurement to "pass/fail criteria" was known at the time of applicant's filing, such as for indicating a scrap wafer to a process engineer.

It would have been obvious to one of ordinary skill in the art at the time of the claimed invention to adopt "electronic circuitry" that "compares" the spectral data "output" in the Battal et al. reference to a "pass/fail criteria," motivated to automate the determination of unacceptable in-process devices being manufactured for time savings and efficiency [MEPEP 2144].

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan Pert whose telephone number is 571-272-1969. The examiner can normally be reached on M-F (7:30AM-3:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ETP
November 11, 2005


EVAN PERT
PRIMARY EXAMINER